## REMARKS

### Election

Applicant confirms election of claims 11-19. Applicant has canceled claims 1-10.

### Claim rejections – 35 USC 103

Claims 11-19 were rejected under 35 USC 103 (a) as being unpatentable over applicant's admitted prior art in view of Kim and Lee.

Present invention:

The present invention deals with the scenario of protecting multiple I/O terminals against ESD pulses. As discussed in the Background to the Invention (page 1, lines 10-20), instead of making use of a complex shunt for each terminal, use is made of a single shunt between the power rails and then each I/O terminal is protected by making use of simple diodes connecting the I/O the simple diode or bipolar structures discussed in the application.

The use of regular two terminal diodes however presents problems as discussed on page 2, lines 11-20.

The present invention addresses this problem of oxide damage to the internal I/O driver while avoiding substantial complexity or cost.

Kim

Kim does not deal with three terminal diodes at all. All of the diodes in Kim are diodes with a single anode and a single cathode, and as discussed in column 3, lines 43-57, each of the diodes 31-36 is a separate diode. Thus Kim also does not teach providing a resistive element between two anodes or two cathodes in a single diode structure.

Lee

Lee deals with a complex circuit for protecting a circuit 11 from ESD pulses on pad 9. The circuit in Lee includes a trigger transistor 20 and a primary device 15 (column 3, line 52), the size and complexity of which is shown in cross-section in Figure 1. This entire structure is connected between the pad and ground to act as a complex stand-alone protection circuit for positive ESD pulses.

Furthermore the resistor 28 in Lee is located between the primary device 15 and secondary device (trigger transistor) 20.

In contrast, the present invention makes use of any standard shunt between power rails and then protects the individual pads or I/O terminals by providing a small, simple solution in the form of a diode between the I/O terminal and the one rail (for positive pulses) and the I/O terminal and the other rail (for negative pulses).

The present invention therefore is not only smaller and cheaper, it also provides a solution for both positive and negative ESD pulses.

Furthermore, in the present invention, the resistive element is not located between the primary device (ESD shunt) and the secondary device (the diode) but provides a voltage drop within the diode itself.

Thus it cannot be said that the simple diode or bipolar transistor solution of the present invention is taught by Lee or Kim and cannot be said to be suggested by Lee or Kim on their own or in combination with the admitted prior art. Neither the admitted prior art nor Kim nor Lee teach or suggest a simple diode with two anodes or cathodes, or a bipolar transistor structure having two bases

Claim 11 has been canceled and the claims 12-14, 17-18 have been amended to clearly distinguish over both Kim and Lee

It is therefore respectfully submitted that all of the claims remaining in the application, as amended are now allowable. Early allowance of the claims is therefore respectfully requested.

Respectfully Submitted,

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